Tristan Sutton

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Objective

U.S. Navy veteran with proven sustained superior performance, adept at working in fast-paced, high-stress environments, an Electrical Engineering student, graduating Spring 2026, with hands-on experience in robotics and satellite AI&T. Eager to pursue a career that leverages my critical thinking and leadership skills. Adaptable and dependable in any situation.

Programming Languages

• C • Python • Labview

Skills

- ROS2 / Nav2
- VS Code, Docker proficiency
- Fundamental Radar Theory
- FPGA Development (Libero/Softconsole)
- Microsoft Project
- Linux (Ubuntu)
- Electronic Assembly/Soldering
- Fusion 360
- Visio / Corel Draw
- Version Control (git)

Professional Experience

Southwest Research Institute San Antonio, TX

Student Engineer-Space Systems April 2025 – Current

- Developed LabVIEW applications using National Instruments PXI hardware (DAQ, DMM, power supplies) to automate EGSE control and data acquisition for functional, thermal vacuum, and vibration testing of FM and EM spacecraft components.
- Designed and fabricated EGSE equipment racks with integrated power distribution and instrumentation, custom interface boxes, and signal conditioning circuits, while authoring test procedures for spacecraft subsystem verification.
- Designed and fabricated flight, flight-like, and non-flight cables for spacecraft integration per NASA-STD-8739 soldering and MIL-STD-22520 crimping specifications.

University of Texas at San Antonio Robotics Laboratory San Antonio, TX

Undergraduate Research Assistant April 2024 – August 2024

- Developed advanced ROS2 navigation packages utilizing SLAM and sensor fusion, integrating Lidar and ultrasonic sensors for precise mapping and obstacle avoidance.
- Engineered robust IoT communication frameworks with MQTT, enabling seamless integration and control of robotic components through sophisticated low-level and high-level control architectures.

United States Navy USS Kidd (DDG 100)

Chief Fire Controlman Aegis – CF Division Leading Chief Petty Officer July 2022 – March 2023

- Supervised a team of 23 Sailors in the upkeep of the Aegis Weapon System
- Coordinated $25 million in system upgrades and installations
- Performed time-critical risk management for personnel and equipment

United States Navy USS Kidd (DDG 100)

A/N SPY1-D(V) Radar Technician March 2015 – July 2022

- Led a team of 6 Sailors in the maintenance of the A/N SPY1-D(V) RADAR suite and auxiliary systems
- Analyzed and troubleshot complex electrical equipment totaling $600 million
- Organized duty personnel schedules encompassing 42 Sailors

Best Buy (Geek Squad) Georgetown, TX
Counter Intelligence Agent June 2012 – January 2015

- Performed advanced diagnostic and repair of computers, phones, TVs, and tablets
- Executed hardware and software repairs on store and client-owned products
- Supervised the storage and transfer of 300 petabytes of client data

Education

University of Texas at San Antonio
B.S. in Electrical Engineering candidate | Graduation Spring 2026
UTSA President's List 2023-2025
GPA 3.97

Relevant coursework	Grade
Analysis & Design – Control Systems	A
Integrated Circuit Design	A
Intro to C Programming	A
Wireless Communications	In Progress
Microcomputer Systems	A
Intelligent Robotics	A

Projects

Banana Bot Fall 2025
Individual Work

- Designed, modeled, and simulated a 2WD autonomous robotic rover using ROS 2 Jazzy Jalisco and Gazebo Harmonic, enabling LiDAR-based maze solving via A* path planning and camera-based YOLO object detection to signal maze completion.

YetiLink (Senior Design) Fall 2025 – Spring 2026
Project Manager

- Led cross-functional engineering team (FPGA, firmware, GUI, and test) through requirements definition, architecture trade studies, and phased execution using a structured work breakdown and milestone schedule.
- Defined system-level requirements and interfaces spanning LVDS telemetry input, HDLC/CCSDS processing, Ethernet output, and Linux-based GUI control.
- Owned system integration and verification planning, coordinating testbed setup, baseline performance characterization, and end-to-end data path validation.

Fimware Engineer

- Implemented and integrated a RISC-V Mi-V softcore processor within a PolarFire FPGA using Libero SoC and SoftConsole to manage runtime configuration, control registers, and system telemetry.
- Designed memory-mapped register interfaces (APB) enabling dynamic control of baud rates, protocol modes, counters, and error reporting from firmware and GUI layers.
- Developed and integrated custom HDL modules for HDLC and non-HDLC data paths, including flag detection, bit unstuffing, CRC checking, FIFO buffering, and Ethernet packetization.