Mohamed Atallah

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Summary

A dedicated Electrical, Electronics and Communications Senior Engineering student at Alexandria University (B.E., expected June 2026) focused on hardware design and digital IC/VLSI. Practical experience with Verilog, PCB design and firmware (C). Additionally I am enthusiastic about hardware acceleration and integrating chip design with ML.

Education

Alexandria University *Alexandria, Egypt*
B.E. in Electrical, Electronics and Communications Engineering *Aug 2021 – June 2026*
GPA 3.13

- **Relevant coursework:** Linear Algebra, Convex Optimization, Digital Logic Design, VHDL, Data Structures, Microprocessors, Operating Systems, Solid State Devices, Digital Communications, Digital Signal Processing.

Si-Vision *Alexandria, Egypt*
Graduation Project in PCIe Gen6 UVM-based VerificationIP *Oct 2025 – present*
Developing and documenting a UVM-based Verification IP (VIP) for the PCIe Gen6 Data Link Layer under industry supervision.

Experience

Summer Trainee — Digital Design for FPGA *Alexandria, Egypt*
NTI (National Telecommunication Institute) *Aug 2025 – Sept 2025*
120-hour technical training program on FPGA digital design.

- Covered fundamentals of VHDL and Verilog for digital system design.
- Learned FPGA design flows including synthesis, implementation, and simulation.
- Introduced to Static Timing Analysis and design constraints.
- Completed a complementary soft skills module on teamwork and communication.

Machine Learning Intern *Alexandria, Egypt*
EME Borg *Aug 2023 – Oct 2023*

- Explored ML subfields and developed CNN models on real datasets.
- Implemented and evaluated models; hands-on experience in model training and testing.

Hardware Intern *Alexandria, Egypt*
Orange Digital Center Egypt *Aug 2023 – Aug 2023*

- PCB design training and exposure to fabrication workflows and CAM tools.
- Laser cutting and 3D printing.

Projects

UVM Based Layered Testbench for an 8bit ALU GitHub
A modular SystemVerilog UVM testbench for verifying an 8-bit TinyALU, featuring constrained random generation, functional coverage, and self-checking scoreboards.

- Targeted and achieved 100% functional coverage on Opcodes (Add, Mul, etc.) and Data boundary values (0x00, 0xFF).

UART Transmitter in Verilog GitHub

Designed a UART transmitter supporting 7/8-bit data, parity control, and 1/2 stop bits.

- Implemented modular components parity generator, frame generator, PISO shift register, and baud rate generator.
- Verified functionality through extensive testbenches and waveform simulation.
- Documented design functionality and test outputs using LaTex

TTL-CMOS IC Tester GitHub

Microcontroller-based tester for TTL and CMOS logic ICs using an ATmega32A MCU.

- Programmed firmware in C with CodeVisionAVR to automate IC testing routines.
- Integrated a Nokia 5110 GLCD to display test results and user controls (push buttons, LEDs, buzzer).
- Supported DIP14 and DIP16 packages via ZIF socket for flexible IC compatibility.
- Documented system architecture, schematics, and usage instructions for reproducibility.

Hand Gesture Classification using CNN and YOLOv8 GitHub

Real-time gesture recognition system deployed on embedded hardware.

- Built a custom CNN from scratch using TensorFlow to classify hand gestures from YOLOv8-detected hand regions.
- Integrated camera input processing and serial communication for gesture-based control.
- Developed an Arduino-based PWM motor demo triggered via serial, with gestures mapped to 20 % speed increments.
- Showcased practical embedded AI control using hand gestures for motor actuation.

Skills

Hardware & Design: Simulation & Testbenches, PCB design, Oscilloscopes, Multimeters, Spectrum Analyzers, Soldering, Laser Cutting

Programming Languages: Verilog, C/C++, Python, MATLAB, Java, JavaScript, Git, LaTeX

Tools: Linux, Xilinx Vivado , QuestaSim, Verilator, GTKWave

Courses

IEEE SSCS Alex SC *Alexandria, Egypt*

Trainee, Chipions'26 Program in Digital IC Design & Verification *Apr 2024 – Oct 2024*

Training in digital IC design, verification, and computer architecture fundamentals.

- Digital IC Design and Verification; organized by IEEE SSCS AUSC.

Udacity *Oct 2021 – Dec 2021*

Nanodegree in Web Development

Front-end development: JavaScript, DOM, Node.js, API integration.

Volunteering

Digital IC Subteam Member *Alexandria, Egypt*

IEEE SSCS AUSC *Mar 2025 – present*

- Support Chipions'27 Digital IC Design training program and the Si-Cast webinar series (technical talks).

Ideaspace Ambassador *Alexandria, Egypt*

EME Borg *Sept 2023 – Dec 2024*

- Helped with community outreach and event support.