Aman Katyal

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Education

Purdue University - West Lafayette   Expected Dec. 2027
B.S. in Computer Engineering   GPA: 3.99/4.0

Technical Experience

Boundary RSS - *AUV Electronics Design Intern*   May 2025 – Aug. 2025
- Architected a hierarchical compute system for swarm-style Autonomous Underwater Vehicles (AUVs), optimizing task distribution between the Raspberry Pi CM5 and NVIDIA Jetson Nano for real-time flight control and AI-driven sensor processing
- Designed complex carrier board schematics to support high-speed peripheral routing, creating custom pin mappings to simplify power delivery and data bus integration for the compute module
- Engineered the schematic design for a custom Power Distribution Board (PDB) to manage battery health monitoring and integrated a passive cooling solution to maintain thermal stability within a waterproof enclosure
- Specified and sourced critical electronic components, compiling a detailed Bill of Materials (BOM) and conducting systems-level trade-off analysis of advanced sensor modalities

Purdue IEEE Remotely Operated Underwater Vehicle (ROV) Team   Aug. 2024 – Present
- Pioneering the full-stack design of a unified test bench board using the RP2350 and STM32, effectively decoupling firmware verification from electrical manufacturing schedules to accelerate software development lifecycles.
- Engineering a custom sensor aggregation PCB that consolidates IMU, depth, and pressure data over I2C/SPI, featuring an automated power multiplexer and a dedicated UART interface for real-time console debugging.
- Consolidated distributed control functions onto a single modular PCB in KiCad, streamlining the firmware workflow and centralizing control of solenoids, PWM servos, and motor drivers for the MATE ROV competition.
- Designed a compact ESC-to-thruster adapter board, utilizing differential pair routing techniques to minimize electromagnetic interference (EMI) and maximize signal integrity for underwater navigation stability.

UVM Verification (Purdue SoCET)   Aug. 2025 – Present
- Architecting a modular, class-based UVM testbench (Agent, Driver, Monitor, Scoreboard) to verify a complex Floating-Point Unit (FPU) for the AFT x09 RISC-V SoC.
- Integrated a C-based floating-point reference model via DPI-C to serve as a self-checking predictor, utilizing TLM analysis ports to facilitate real-time, cycle-accurate comparison of the DUT against the RTL.
- Executed a comprehensive verification plan targeting IEEE 754 corner cases (rounding modes, denormals) and closed functional coverage holes using Constrained Random Verification (CRV) in AMD Vivado.
- Developed Tcl automation scripts to programmatically generate project structures and configure simulation environments, establishing a reproducible "push-button" workflow for the design team.

Projects

Microcontroller Dueling System with ML-Enabled Gesture Input   May 2025 – Aug. 2025
- Engineered a full-stack embedded system utilizing the RP2350's dual-core architecture, designating one core to handle high-frequency IMU polling and TensorFlow Lite inference (<5ms latency, 96% accuracy), while offloading peripheral I/O and game logic to the second core.
- Implemented a robust line-of-sight Infrared (IR) communication protocol using PWM encoding for transmission and GPIO interrupts for non-blocking signal reception, utilizing a packet redundancy scheme to validate hits on a custom wearable receiver.
- Designed and fabricated a custom PCB integrating an I2C haptic driver and PIO-driven RGB LED matrix, housing the electronics in custom 3D-printed enclosures to create a fully functional, ergonomic hardware prototype.

ESP32 Universal Game Controller Bridge   May 2025 – Aug. 2025
- Developed a cost-effective controller bridge on the ESP32-S3 using ESP-IDF (C++), engineering a mechanism to intercept Bluetooth packets from third-party controllers and translate them into Nintendo Switch-compatible USB HID reports.
- Optimized the dual-stack Bluetooth/USB architecture to achieve verified sub-30ms latency, systematically debugging critical heap fragmentation issues and memory leaks to ensure stable performance during extended gaming sessions.

Verification & Digital Design: UVM, SystemVerilog, RISC-V, DPI-C, Tcl Scripting, APB/AHB, AMD Vivado, QuestaSim
Electronics & PCB Design: KiCad (Schematic & Layout), Differential Pairs, I2C/SPI/UART/RS-485, Oscilloscopes, Logic Analyzers
Programming & Firmware: Embedded C/C++, Python, MATLAB, Microcontrollers (ESP32, STM32, RP2350), Git, Linux