SHARON BIKOBO

Final-Year Engineering Student – Junior RF / Analog Design Engineer
Grenoble, France

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Summary

Final-year engineering student with **3 years of industry experience** across **RF and analog IC design** and **design automation**. Strong exposure to the full design cycle from **schematic** to **post-layout verification** (DRC/LVS/PEX) and **EM/circuit correlation**. Hands-on with **Cadence Virtuoso** (Spectre/RFPro/SKILL) and **Keysight ADS** on RF building blocks and mixed-signal interfaces.

Education

- **Bachelor's and Master's Degree in Physics and Microelectronics Systems** *Sept. 2023 – Sept. 2026*
  CPE Lyon – Engineering School of Chemistry, Physics, and Electronics (Lyon, France)
  - **RF & Analog Design:** Designed and simulated **LNA, RF mixer, three-stage amplifier, and OTA** in **Cadence Virtuoso**; transceiver-level exploration with **ADISimRF** and **PCB layout** in **KiCad**.
  - **Digital & Embedded:** Implemented **FPGA/CPLD** designs in **VHDL**; automated HDL conversions using **Python**; embedded SDR prototype using **STM32** and **GNU Radio**.
- **Intensive years study course in physics and engineering science** *Sept. 2021 – June 2023*
  Classes préparatoires associées CPE Lyon – Institution des Chartreux (Lyon, France)

Professional Experience

- **Research Intern – Neuromorphic / Analog IC Design** *Jul. 2025 – Sept. 2025*
  INESC MN (Lisbon, Portugal)
  - Designed and simulated neuromorphic/analog circuit blocks to mimic **neuron/synapse** dynamics in **Spectre** (Cadence).
  - Developed a sensor-interface concept leveraging **pseudo-resistors** to achieve ultra-low-frequency behaviors and high effective time constants.
  - Performed **parametric exploration** (bias, process-style variations when applicable) to evaluate operating margins, stability, and trade-offs.
- **Apprentice Engineer – multidisciplinary teams (RF, Analog, Digital)** *Jan. 2023 – Sept. 2026*
  Asygn – Service provider in IC, RF, Inertial sensors and AI (Grenoble, France)

  RF Team *Oct. 2024 – Sept. 2025*
  - Created **5 parameterized layout cells** using **SKILL scripting** for RF passive components (transmission lines, shielded/unshielded spiral inductors) in **Cadence Virtuoso**.
  - Optimized X-band (8.5 GHz) interconnects via **EM simulation**, achieving **50 Ω impedance matching** and **27% improved loss margin**; developed **S-parameter to RLCG extraction workflow** validated with **-32.6 dB input return loss**.
  - Designed **X-band Wilkinson power divider** from schematic through **post-layout verification** (LVS, parasitic extraction), meeting all RF performance targets within $<$**0.25 mm**^{2} constraint.

  Digital Design Team *Jun. 2024 – Oct. 2024*
  - Developed digital interfaces for mixed-signal systems, focusing on robust integration and validation.
  - Implemented **SPI communication** between **STM32 microcontroller** and **FPGA**; supported bring-up and interface verification.
  - Automated RTL/firmware-related tasks using **Python** and contributed to **SystemVerilog** register-level optimizations.

  Analog Design Team *Jan. 2024 – Jun. 2024*
  - Designed a **PMOS LDO regulator** (3.3 V → 3.0 V, 10 μA–1 mA load) with a **2-stage Miller-compensated** error amplifier in **Cadence Virtuoso**.
  - Achieved stability and performance targets (**75–94° phase margin**, **23–31 dB gain margin**, **200 mV dropout @ 0.91 mA**, **14 μA** quiescent current).
  - Validated across operating conditions and transients: worst-case line regulation of **6 mV** for a 165 mV input step; checked key corners for robustness.

Skills

- **Design Tools & Software:** Cadence Virtuoso (Spectre, RFPro, SKILL), Keysight ADS, LTspice, KiCad, MATLAB/Simulink, LaTeX.
- **Programming:** Python, VHDL, SystemVerilog, C, SKILL scripting, Assembly.
- **Technical Expertise:** RF/Analog IC design, Mixed-signal circuit design, EM simulation, Layout (DRC/LVS/PEX), RTL design, PCB design.
- **Languages:** French (Native), English (Advanced – CEFR C1).