VAHE OHIHOIN

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https://issuu.com/vohihoin/docs/vahe_ohihoin_project_portfolio

EDUCATION

University of Wisconsin-Madison
Bachelor of Science, ***Computer Engineering*** | Junior standing
Additional Majors: ***Computer Science***, ***Mathematics*** | GPA: ***4.0/4.0*** | Dean's List (2/2)
Selected Coursework: Digital Design Fundamentals, Intro. to Microprocessor Systems, Matrix Methods in Machine Learning
Scholarships and Recognitions
Mercile J. Lee -Chancellor, STAR Engineering Scholarship, *Wisconsin Merit*, *National Merit Commended Scholar, ACT – 36/36*

ENGINEERING WORK EXPERIENCE

Horseshoe Beverage Company, Neenah WI.
Controls & Automation Intern, May – August 2025

- Engineered and implemented a new PLC-based wastewater pH control system using Allen-Bradley and Hach PLCs.
- Crafted interactive FactoryTalk HMI and Ignition Perspective interfaces for system control and plant monitoring.
- Integrated a CIP (clean-in-place) system into our server-based AVEVA PI data collection system and worked with a a fellow intern to commission and perform IQ-OQ-PQ on the system.
- Programmed a PLC routine to automatically start and manage expiration timers when new product is brought into the facility.

Civil Engineering Department, University of Texas, San Antonio - github.com/Vohihoin/UTSA_Internship
Software Engineering Intern – Computer Vision, July - August 2024

- Delivered a real-time computer vision application to evaluate the safety of workers in a construction site through live video footage and raise alarms if a worker is positioned unsafely.
- Programmed the application in python using OpenCV, mediapipe and YOLO models. The program evaluates the pose of construction workers using live webcam footage and assigns a safety score using the REBA ergonomic algorithm.

PROJECT EXPERIENCE

Embedded Alarm Clock
Embedded C, ARM Architecture, Intro to Microprocessor Systems Class Project F25

- Developed an embedded alarm clock application on a PSoC6 Cortex-M development board, featuring LCD time display, user-configurable time and alarm, and buzzer alerts.
- Programmed bare-metal firmware including custom peripheral drivers, timer interrupts for button debouncing, and PWM control.

Digital Alarm Clock - github.com/Vohihoin/AlarmClock
System Verilog, FPGA implementation, PCB Design, May 2025 - Present.

- Designed, developing, & implementing an FPGA based Alarm Clock. Logic written in System Verilog, tested in ModelSim, compiled in Quartus Prime (24.1 std) and run on an Altera Cyclone IV.
- Creating PCB in Altium Designer to connect to FPGA and display the time on 7-segment-displays.

FPGA-Based Machine Learning Motion Detection System - github.com/Vohihoin/ECE352
System Verilog, FPGA implementation, Digital Design and Fundamentals Class Project S25.

- Implemented an FPGA-based machine learning system for classifying a user's motion based on accelerometer data.
- Wrote the logic in System Verilog, tested it in ModelSim, compiled in Quartus and ran on an Altera Cyclone FPGA.
- Created a Serial-Shift-Register to collect data from the accelerometer, and a complex FSM to control the calculation cycle.

Data structure Database - github.com/Vohihoin/DataStructureDatabase
Java, April 2025 - present

- Developed efficient and versatile implementations of graphs, skiplists, tries, red-black trees, hashtables, priority-queues.
- Pioneered an adjacency-list graph implementation, that used hash tables instead of lists, with nodes being used as keys to find edges to improve efficiency for graphs that are dense in edges.

EXTRACURRICULAR INVOLVEMENT

National Society of Black Engineers (NSBE) – attend national & regional conferences, **Life Center**, **Cru**

SKILLS

Programming Languages: C (Systems & Embedded), System Verilog, Java, Python, Ladder Logic, LC3-Assembly, Arduino, MySQL. Hardware Design Tools: Altium Designer, LTSpice, Quartus, ModelSim, Altera FPGAs. Automation: Allen-Bradley RSLogix and CCW Suite, IDEC Automation. Software Dev Tools: Git, Github, Google Cloud Provider, Linux Bash. Libraries: OpenCV, Mediapipe, JavaFX, MySQL JDBC.